In the Claims:

Please amend Claims 1, 8, 15, and 22 as follows.

1. (ONCE AMENDED) A method of forming source/drain regions, comprising the steps of:

providing a semiconductor integrated circuit wafer having source/drain regions;

providing an ion implant apparatus;

placing a phosphorous ion source in said ion implant apparatus;

adjusting said ion implant apparatus so that said ion implant apparatus produces an ion beam comprising P_2^+ ions, wherein said ion beam has a beam density and a beam energy;

implanting P_2^+ ions into said source/drain regions of said integrated circuit wafer using a single ion implantation step and said ion implant beam; and

annealing said integrated circuit wafer having P_2^+ ions implanted at an anneal temperature for an anneal time.

8. (ONCE AMENDED) A method of forming source/drain regions, comprising the steps of:

providing a semiconductor integrated circuit wafer having source/drain regions;

providing an ion implant apparatus;

placing an arsenic ion source in said ion implant apparatus;

adjusting said ion implant apparatus so that said ion implant apparatus produces an ion beam comprising As_2^+ ions, wherein said ion beam has a beam density and a beam energy;

implanting As_2^+ ions into said source/drain regions of said integrated circuit wafer using a single ion implantation step and said ion implant beam; and

annealing said integrated circuit wafer having As_2^+ ions implanted at an anneal temperature for an anneal time.

15. (ONCE AMENDED) A method of doping a polysilicon electrode, comprising the steps of:

providing a semiconductor integrated circuit wafer having a polysilicon electrode formed thereon;

providing an ion implant apparatus;

placing a phosphorous ion source in said ion implant apparatus;

adjusting said ion implant apparatus so that said ion implant apparatus produces an ion beam comprising P_2^+ ions, wherein said ion beam has a beam density and a beam energy;

implanting P_2^+ ions into said polysilicon electrode using a single ion implantation step and said ion implant beam; and

annealing said integrated circuit wafer having P_2^+ ions implanted at an anneal temperature for an anneal time.